REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV																					
PAGE																					
REV STATUS OF PAGES	**REV**																				
	PAGE	1	2	3	4	5	6	7	8	9	10										

PMIC N/A

PREPARED BY
Phu H. Nguyen

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil/

Original date of drawing
YY MM DD
12-11-20

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

TITLE

MICROCIRCUIT, DIGITAL-LINEAR, 16-BIT,
1 MSPS PulSAR ADC, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/12640

REV

PAGE 1 **OF** 10

AMSC N/A

5962-V026-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16-bit, 1 MSPS PulSAR ADC microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12640	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7980-EP	16-bit, 1 MSPS PulSAR ADC

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	10	JEDEC MO-187-BA	Mini Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Analog inputs: IN+, IN- to GND	-0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply voltage:	
REF, V_{IO} to GND	-0.3 V to +6 V
V_{DD} to GND	-0.3 V to +3 V
V_{DD} to V_{IO}	+3 V to -6 V
Digital inputs to GND	-0.3 V to V_{IO} + 0.3 V
Digital outputs to GND	-0.3 V to V_{IO} + 0.3 V
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
θ_{JA} Thermal impedance (Case outline X)	200°C/W
θ_{JC} Thermal impedance (Case outline X)	44°C/W
Lead temperature:	
Vapor phase (60 sec)	215°C
Infrared (15 sec)	220°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Load circuit for digital interface timing. The load circuit for digital interface timing shall be as shown in figure 3.

3.5.4 Voltage levels for timing. The voltage levels for timing shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions V_{DD} = 2.5 V, V_{REF} = 5.0 V 2.3 V ≤ V_{IO} ≤ 5.5 V -55°C ≤ T_A ≤ +125°C unless otherwise noted	Limits			Unit
			Min	Typ	Max	
Resolution			16			Bits
Analog input						
Voltage range		IN+ - IN-	0		V_{REF}	V
Absolute input voltage		IN+	-0.1		V_{REF} + 0.1	V
		IN-	-0.1		+0.1	
Analog input CMRR		f_{IN} = 100 kHz		60		dB
Leakage current @ 25°C		Acquisition phase		1		nA
Accuracy						
No missing codes			16			Bits
Differential linearity error		REF = 5 V	-0.9	±0.4	+0.9	LSB 2/
		REF = 2.5 V		±0.55		
Integral linearity error		REF = 5 V	-1.5	±0.6	+1.5	
		REF = 2.5 V		±0.65		
Transition noise		REF = 5 V		0.6		
		REF = 2.5 V		1.0		
Gain error, T_{MIN} to T_{MAX} 3/				±2		
Gain error temperature drift				±0.35		ppm/°C
Zero error, T_{MIN} to T_{MAX} 3/			-0.62	±0.08	+0.62	mV
Zero temperature drift				0.54		ppm/°C
Power supply sensitivity		V_{DD} = 2.5 V ± 5%		±0.1		LSB 2/
Throughput						
Conversion rate		V_{IO} ≥ 2.3 V up to 85°C, V_{IO} ≥ 3.3 V above 85°C up to 125°C	0		1	MSPS
Transient response		Full scale step			290	ns
AC accuracy						
Dynamic range		V_{REF} = 5V		92		dB 4/
		V_{REF} = 2.5V		87		
Oversampled dynamic range		f_o = 10 kSPS		111		
Signal to Noise Ratio,	SNR	f_{IN} = 10 kHz, V_{REF} = 5 V		91		
		f_{IN} = 10 kHz, V_{REF} = 2.5 V		86.5		
Spurious Free Dynamic Range,	SFDR	f_{IN} = 10 kHz		-110		
Total Harmonic Distortion,	THD	f_{IN} = 10 kHz		-114		
Signal to (Noise +Distortion),	SINAD	f_{IN} = 10 kHz, V_{REF} = 5 V		91.5		
		f_{IN} = 10 kHz, V_{REF} = 2.5 V		87.0		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions V_{DD} = 2.5 V, V_{REF} = 5.0 V 2.3 V ≤ V_{IO} ≤ 5.5 V -55°C ≤ T_A ≤ +125°C unless otherwise noted	Limits			Unit
			Min	Typ	Max	
Reference						
Voltage range			2.4		5.1	V
Load current		1 MSPS, REF = 5 V		330		µA
Sampling dynamics						
-3 dB input bandwidth				10		MHz
Aperture delay		V_{DD} = 2.5 V		2.0		ns
Digital inputs						
Logic level	V_{IL}	V_{IO} > 3 V	-0.3		0.3 x V_{IO}	V
	V_{IH}	V_{IO} > 3 V	0.7 x V_{IO}		V_{IO} + 0.3	
	V_{IL}	V_{IO} ≤ 3 V	-0.3		0.1 x V_{IO}	
	V_{IH}	V_{IO} ≤ 3 V	0.9 x V_{IO}		V_{IO} + 0.3	
	I_{IL}		-1		+1	µA
	I_{IH}		-1		+1	
Digital outputs						
Data format		Serial 16 bits straight binary				
Pipeline delay		Conversion results available immediately after completed conversion				
	V_{OL}	I_{SINK} = 500 µA			0.4	V
	V_{OH}	I_{SOURCE} = -500 µA	V_{IO} – 0.3			
Power supply						
V_{DD}			2.375	2.5	2.625	V
V_{IO}		Specified performance	2.3		5.5	
V_{IO} range			1.8		5.5	
Standby current 5/ 6/		V_{DD} and V_{IO} = 2.5 V, T_A = 25°C		0.35		nA
Power dissipation		10 kSPS throughput		70		µW
		1 MSPS throughput		7.0	10	mW
Energy per conversion				7.0		nJ/sample
Temperature range						
Specified performance		T_{MIN} to T_{MAX}	-55		+125	°C

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2.37 V ≤ V_{DD} ≤ 2.63 V 3.3 V ≤ V_{IO} ≤ 5.5 V -55°C ≤ T_A ≤ +125°C unless otherwise noted	Limits			Unit
			Min	Typ	Max	
Timing specifications (see FIGURE 2 and 3 for load condition)						
Conversion time: CNV rising edge to data available	t_{CONV}		500		710	ns
Acquisition time	t_{ACQ}		290			
Time between conversions	t_{CYC}		1000			
CNV pulse width ($\overline{CS}$ Mode)	t_{CNVH}		10			
SCK period ($\overline{CS}$ Mode)	t_{SCK}	V_{IO} above 4.5 V	10.5			
		V_{IO} above 3 V	12			
		V_{IO} above 2.7 V	13			
		V_{IO} above 2.3 V	15			
SCK period (chain mode)	t_{SCK}	V_{IO} above 4.5 V	11.5			
		V_{IO} above 3 V	13			
		V_{IO} above 2.7 V	14			
		V_{IO} above 2.3 V	16			
SCK low time	t_{SCKL}		4.5			
SCK high time	t_{SCKH}		4.5			
SCK falling edge to data remains valid	t_{HSDO}		3			
SCK falling edge to data valid delay	t_{DSDO}	V_{IO} above 4.5 V			9.5	
		V_{IO} above 3 V			11	
		V_{IO} above 2.7 V			12	
		V_{IO} above 2.3 V			14	
CNV or SDI low to SDO D15 MSB valid ($\overline{CS}$ Mode)	t_{EN}	V_{IO} above 3 V			10	
		V_{IO} above 2.7 V			15	
CNV or SDI high or last SCK falling edge to SDO high impedance ($\overline{CS}$ Mode)	t_{DIS}				20	
SDI valid setup time from CNV rising edge	$t_{SSDICNV}$		5			
SDI valid hold time from CNV rising edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$		2			
SDI valid hold time from CNV rising edge (Chain Mode)	$t_{HSDICNV}$		0			
SCK valid setup time from CNV rising edge (Chain mode)	$t_{SSCKCNV}$		5			
SCK valid hold time from CNV rising edge (Chain Mode)	$t_{HSCKCNV}$		5			
SDI valid setup time from SCK falling edge (Chain mode)	$t_{SSDISCK}$		2			
SDI valid hold time from SCK falling edge (Chain Mode)	$t_{HSDISCK}$		3			
SDI high to SDO high (Chain mode with Busy Indicator)	$t_{DSDOSDI}$				15	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ LSB means least significant bit. With the 5 V input range, 1 LSB is 76.3 µV.

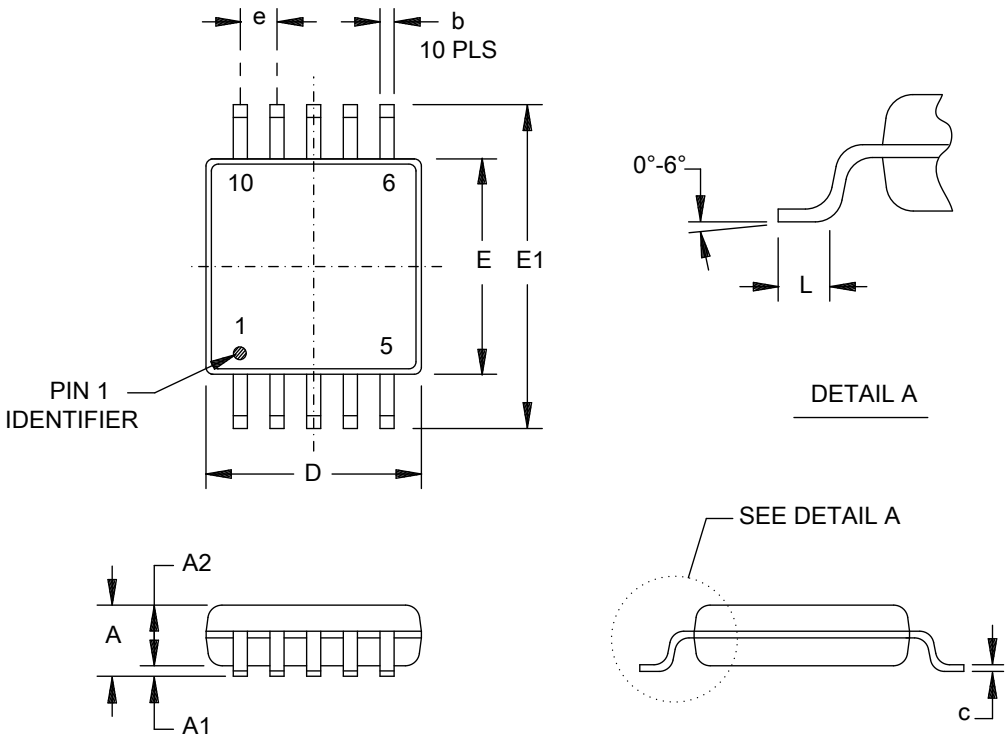
3/ These specifications include full temperature range variation, but not the error contribution from the external reference.

4/ All specifications in dB are referred to a full scale input FSR. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

5/ With all digital inputs forced to VIO or GND as required.

6/ During the acquisition phase.

Case X



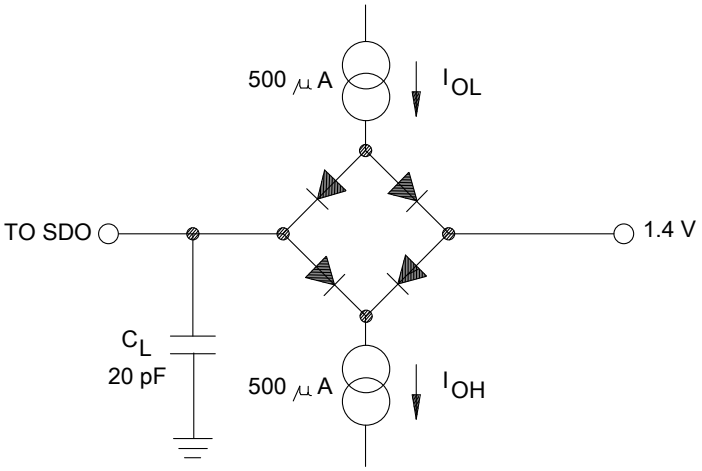
Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.10	D/E	2.90	3.10
A1	0.05	0.15	E1	4.65	5.15
A2	0.75	0.95	e	0.50 BSC	
b	0.15	0.30	L	0.40	0.70
c	0.13	0.23			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-187-BA.

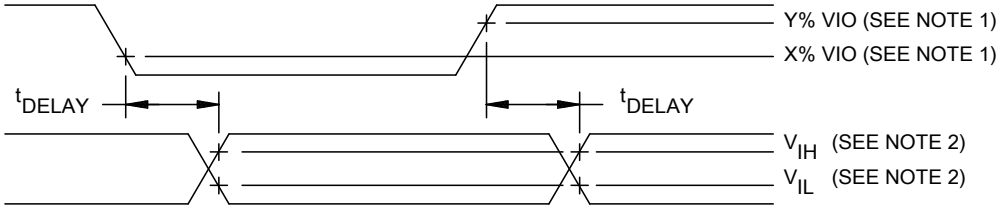
FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	REF	10	VIO
2	V_{DD}	9	SDI
3	IN+	8	SCK
4	IN-	7	SDO
5	GND	6	CNV

FIGURE 2. Terminal connections.



IGURE 3. Load circuit for digital interface timing.



NOTES:
1. For $V_{IO} \leq 3.0$ V, X = 90 and Y = 10; For $V_{IO} > 3.0$ V X = 70 and Y = 30.
2. Minimum V_{IH} and maximum V_{IL} used. See Digital Inputs specifications in table I.

FIGURE 4. Voltage levels for timing.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12640-01XE	24355	AD7980SRMZ-EP-RL7 2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Z = RoHS compliant part

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106